REMARKS

In the Office Action, the Examiner noted that claims 1-28 are pending in the application, of which claims 12-17 and 24-28 are withdrawn from consideration. The Examiner rejected claims 1-5, 7-19, 18-20, and 22, and objected to claims 6, 11, 21, and 23. By this response, claims 12-17 and 24-28 remain withdrawn subject to possible rejoinder. Claims 4 and 18-19 are amended. In view of the following discussion, the Applicant submits that none of the claims now pending in the application are anticipated under the provisions of 35 U.S.C. §102 or obvious under the provisions of 35 U.S.C. §103. Thus, the Applicant believes that all of these claims are now in condition for allowance.

I. Restriction Requirement

The Applicant affirms the election of claims 1-11 and 18-23 (referred to as Group I) with traverse. Claims 12-17 and 24-28 have been withdrawn without prejudice.

II. Objections

A. Claim 1

The Examiner objected to the phrase "to minimize critical connections" in claim 1 as being unclear. The Examiner stated that the phrase does not clearly define whether the number of critical connections is to be minimized, or the timing delay of the critical connections.

The Applicant submits that the step "placing the components of the circuit design to minimize critical connections" is clear. The phrase "minimize critical connections" is broad enough to cover both minimization of timing delay and number of critical connections and is clear to those skilled in the art. Notably, the components of the circuit design are placed such that the timing delays of critical connections are minimized. In some cases, the timing delays may be minimized such that the connections are no longer critical. In this manner, the number of critical connections is also minimized. Accordingly, Applicants respectfully request that the object to claim 1 be withdrawn.

B. Claims 4 and 19

The Examiner objected to the phrase "combining slices that share control signals and clock sources" in claims 4 and 19 as being unclear. The Examiner posed the question of what circuit is formed by the combined slices. The Applicant has amended claims 4 and 19 to state that the slices are combined to form a combined slice. The Applicant contends that claims 4 and 19, as amended, are clear. Accordingly, the Applicant respectfully requests that the objection to claims 4 and 19 be withdrawn.

C. Claims 6, 11, 21, and 23

The Examiner has objected to dependent claims 6, 11, 21, and 23 as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form. Applicants thank the Examiner for indicating allowable subject matter, but believe independent claims 1 and 18, from which these dependent claims depend, are allowable over the prior art of record for the reasons set forth below. Thus, Applicants contend that claims 6, 11, 21, and 23 should distinguish over the prior art of record, since each claim depends from independent claims 1 or 18. Therefore, Applicants respectfully request that the objection to claims 6, 11, 21, and 23 be withdrawn.

III. Rejection of Claims Under 35 U.S.C. §102

The Examiner rejected claims 1-3, 7, 10, and 18 as being anticipated by Wu (United States patent 6,813,754, issued November 2, 2004). The rejection is respectfully traversed.

More specifically, the Examiner stated that Wu discloses packing components of a circuit design that are dependent upon an architecture of the circuit design. (Office Action, p. 4). The Examiner further stated that Wu discloses assigning initial locations to components of a circuit design, clustering a plurality of components according to design constraints, and placing the components to minimize critical connections. (Office Action, p. 5). The Examiner concluded that Wu anticipates Applicant's invention recited in claim 1.

Wu generally teaches a place-and-route process for programmable logic devices (PLDs). (See Wu, Abstract). In particular, logic cells/clusters are packed using a packing algorithm that optimizes local connectivity between cells and/or clusters and attempts to place a group of related clusters into a single block. (Wu, col. 3, lines 25-32; step 204 in FIGs. 2 and 3). The packed blocks are then placed onto CLBs in the device (Wu, col. 3, lines 32-35; step 206 in FIGs. 2 and 3). Wu discloses that one or more nodes of the most critical K paths are moved to one or more different CLBs in order to reduce delay. (Wu, col. 4, lines 29-32; step 302, FIG. 3; step 404, FIG. 4). After the node relocation, interconnections are routed between the CLBs. (Wu, lines 42-44; step 208, FIGs. 2 and 3).

Wu, however, does not teach each and every element of Applicant's claim 1. Namely, Wu does not teach or suggest "clustering a plurality of components of the circuit design according to design constraints." (Applicant's claim 1). In Applicant's claim 1, components of a circuit design are packed dependent upon an architecture of the circuit design and assigned initial locations. Some of the components of the circuit design are then clustered according to design constraints. The components are then placed to minimize critical connections. Thus, Applicant's claim 1 recites two separate steps where components are packed or clustered.

Wu only teaches a single step of packing of logic cells/clusters. Wu does not teach or suggest clustering logic cells/clusters according to design constraints after the packed blocks are placed on CLBs and before nodes are re-placed to reduce delays. Rather, Wu discloses a process whereby logic cells/clusters are packed into blocks, the blocks are placed, and some nodes are re-placed to reduce delay. Wu is devoid of any teaching or suggestion of a second packing or clustering step.

"Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim." Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 221 USPQ 481, 485 (Fed. Cir. 1984). Since Wu does not teach a second packing or clustering step, Wu does not teach each and every element of Applicant's claim 1 as arranged therein. Accordingly, Wu does not anticipate Applicant's invention recited in claim 1.

Claim 18 includes features similar to those of claim 1 emphasized above. For the same reasons set forth above, the Applicant contends that Wu does not anticipate the invention of claim 18. Finally, claims 2-3, 7, and 10 depend, either directly or indirectly, from claim 1 and recite additional features therefor. Since Wu does not anticipate Applicants' invention as recited in claim 1, dependent claims 2-3, 7, and 10 are also not anticipated and are allowable. Therefore, the Applicant contends that claims 1-3, 7, 10, and 18 are not anticipated by Wu and, as such, fully satisfy the requirements of 35 U.S.C. §102.

IV. Rejection Of Claims Under 35 U.S.C. §103

A. Claims 4, 8, and 19

The Examiner rejected claims 4, 8 and 19 as being unpatentable over Wu in view of Chen (United States patent 5,475,830, issued December 12, 1995). The rejection is respectfully traversed.

More specifically, the Examiner conceded that Wu does not teach combining slices that share control signals and clock sources such that the total number of components of the combined slice does not exceed a threshold number of components. (Office Action, p. 7). The Examiner stated, however, that Chen teaches a method of clustering storage instances that share data paths and clock paths such that each cluster should include a number of components no larger than a threshold size. (Office Action, p. 7). The Examiner concluded that it would have been obvious to combine the clustering step of Wu with that of Chen.

Chen generally teaches implementing integrated circuit designs into a plurality of clocked and un-clocked re-programmable logic circuits. Clusters are formed in the target logic circuit, which are implemented into the clocked and un-clocked re-programmable circuits. (See Chen, Abstract).

Claims 4, 8, and 19 depend from claims 1 and 18 and recite additional features therefor. The cited references, either singly or in any permissible combination, do not teach, suggest, or otherwise render obvious Applicant's invention recited in claims 1 and 18. Namely, the combination of Wu and Chen does not teach or suggest clustering a plurality of components of the circuit design according to design

constraints. As discussed above, Wu is devoid of any teaching or suggestion of a second clustering step. Chen is also devoid of two separate packing and clustering steps. Thus, no conceivable combination of Wu and Chen renders obvious Applicant's invention of claims 1 and 18. Therefore, Applicants contend that claims 4, 8, and 19, which depend from claims 1 and 18, are patentable over the combination of Wu and Chen and, as such, fully satisfy the requirements of 35 U.S.C. §103.

B. Claims 5, 9, 20, and 22

The Examiner rejected claims 5, 9, 20, and 22 as being unpatentable over Wu in view of Russo ("A computer-based-design Approach to Partitioning and Mapping of Computer Logic Graphs," Proc. IEEE, vol. 60, no. 1, Jan. 1972). The rejection is respectfully traversed.

More specifically, the Examiner conceded that Wu does not disclose including slices in a CLB if the total number of inputs and outputs of the resulting CLB does not exceed a threshold number of inputs and outputs. (Office Action, p. 8). The Examiner stated, however, that Russo discloses partitioning and mapping of logic blocks wherein one constraint required for a partition of logic blocks to be acceptable is that a total number of external connections should be equal or less than an external connection capacity. (Office Action, p. 8). The Examiner concluded that it would have been obvious to combine the clustering step of Wu with that of Russo.

Claims 5, 9, 20, and 22 depend from claims 1 and 18 and recite additional features therefor. The cited references, either singly or in any permissible combination, do not teach, suggest, or otherwise render obvious Applicant's invention recited in claims 1 and 18. Namely, the combination of Wu and Russo does not teach or suggest clustering a plurality of components of the circuit design according to design constraints. As discussed above, Wu is devoid of any teaching or suggestion of a second clustering step. Russo is also devoid of two separate packing and clustering steps. Thus, no conceivable combination of Wu and Russo renders obvious Applicant's invention of claims 1 and 18. Therefore, Applicants contend that claims 5, 9, 20, and 22, which depend from claims 1 and 18, are patentable over the

combination of Wu and Russo and, as such, fully satisfy the requirements of 35 U.S.C. §103.

CONCLUSION

Thus, the Applicant submits that none of the claims presently in the application are anticipated under the provisions of 35 U.S.C. §102 or obvious under the provisions of 35 U.S.C. §103. Consequently, the Applicant believes that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If, however, the Examiner believes that there are any unresolved issues requiring any adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Kim Kanzaki at (408) 879-6149 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on January 3, 2006.

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